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APPENDIX A

Figure 19 is a schematic diagram illustrating an example of an input stage of an offsetable differential receiver in accordance with an embodiment of the invention. A differential input signal is coupled to an input 1901 at a gate of a first input transistor 1903 and to an input 1902 at a gate of a second input transistor 1904. A source of the first input transistor 1903 and a source of the second input transistor 1904 are coupled to a first terminal 19119 of current source 19120. A second terminal 19213 of current source 19120 is coupled to ground.